IN THE CLAIMS

1.   (Currently Amended) A method for capturing hardware trace data, the method comprising:

defining a wrap-back address space;

during compression mode, storing trace data circularly in the wrap-back address space; and

upon exiting compression mode, establishing a write address for further trace data such that trace data prior to exiting compression mode is maintained;

wherein said establishing said write address includes retrieving a jump-to address outside of said wrap-back address space and writing said further trace data to said jump-to address space.

2.   (Canceled)

3.   (Original) The method of claim 1 wherein:

said establishing said write address includes incrementing a current write address within said wrap-back address space.

4.   (Original) The method of claim 1 wherein:

said wrap-back address space holds N cycles of trace data;

said storing trace data including maintaining a wrap-back flag that changes value every N cycles during compression.

5.   (Original) The method of claim 4 further comprising:

reordering said trace data from said wrap-back address space in response to said wrap-back flag.

6.   (Original) The method of claim 1 further comprising:

providing a user programmable sensitivity setting for each unit generating trace data, each said unit generating an idle signal in response to said sensitivity settings;

entering said compression mode during which said trace data is compressed upon a plurality of said units generating said idle signal.

7. (Currently Amended) A system for capturing hardware trace data, the system comprising:

trace arrays including a wrap-back address space;

trace controls including a trace data write address register containing an address within said trace arrays for trace data;

a wrap-back address decrementor;

a jump-to address incrementor;

during compression mode, said trace controls controlling said address within said write address register by storing an output of said wrap-back address decrementor in said write address register to store trace data circularly in said wrap-back address space;

upon exiting compression mode, said trace controls establishing said address within said write address register for further trace data such that trace data prior to exiting compression mode is maintained; said trace controls receiving a jump-to address from said jump-to address incrementor, said trace controls writing said jump-to address to said write address register, said further trace data being written to a jump-to address space.

8. (Canceled)

9. (Original) The system of claim 7 further comprising:

an address incrementor;

said trace controls receiving an incremented address from said address incrementor;

said trace controls writing said incremented address to said write address register, said further trace data being written to an incremented address space within said wrap-back address space.

10. (Original) The system of claim 7 wherein:

said wrap-back address space holds N cycles of trace data;

said trace controls maintaining a wrap-back flag that changes value every N cycles during compression.

11.   (Original) The system of claim 10 wherein:

said trace controls reorder said trace data from said wrap-back address space in response to said wrap-back flag.

12.   (Original) The system of claim 7 further comprising:

a user programmable sensitivity setting for each unit generating trace data, each said unit generating an idle signal in response to said sensitivity settings;

compression controls placing said trace controls in said compression mode during which said trace data is compressed upon a plurality of said units generating said idle signal.

13.   (Original) A method of controlling compression of trace data in a processor, the method comprising:

providing a user programmable sensitivity setting for each unit generating trace data, each said unit generating an idle signal in response to said sensitivity settings;

entering a compression mode during which said trace data is compressed upon a plurality of said units generating said idle signal.

14.   (Original) The method of claim 13 wherein:

said units generate a start signal initiating trace data capture;

maintaining a count of cycles without receiving a start signal from one of said units;

entering said compression mode when said count of cycles reaches a programmed limit.

15.   (Original) The method of claim 14 further comprising:

resetting said count of cycles to cease said compression mode when one of said units ceases generating said idle signal.

16.   (Original) A system for controlling compression of trace data from units in a processor, the system comprising:

a user programmable sensitivity setting for each unit generating trace data, each said unit generating an idle signal in response to said sensitivity settings;

compression controls generating a compression signal in response to a plurality of said units generating said idle signal; and

trace controls entering a compression mode in response to said compression signal, during which said trace data is compressed.

17.   (Original) The system of claim 16 wherein:

said units generate a start signal initiating trace data capture;

said compression controls including a counter maintaining a count of cycles without receiving a start signal from one of said units;

said compression controls generating said compression signal when said counter reaches a programmed limit.

18.   (Original) The system of claim 17 wherein:

said counter resets to cease said compression signal when one of said units ceases generating said idle signal.

19.   (Original) A method of pre-detecting a hardware hang in a processor, the method comprising:

maintaining a count of a number of cycles in a predefined time interval without an instruction being completed;

detecting a pre-hang condition if said count is within N counts of a hang limit;

initiating trace capture in response to detecting said pre-hang condition; and

detecting a hang condition if said count equals said hang limit.

20.   (Original) A system for pre-detecting a hardware hang in a processor, the system comprising:

a hang counter maintaining a count of a number of cycles in a predefined time interval without an instruction being completed;

a pre-hang detector   detecting a pre-hang condition if said hang counter is within N counts of a hang limit;

a pre-hang detect latch initiating trace capture in response to said pre-hang detector detecting a pre-hang condition; and

a hang detector resetting said pre-hang detect latch if said hang counter equals said hang limit.